

REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C. § 103(a) Rejections

Examiner rejected claims 1-12, 16, 29, 30 and 32 under 35 U.S.C. § 103(a) as being unaparentable by U.S. Patent No. 6,063,677 (hereinafter "Rodder") in view of U.S. Patent 5,937,300 (hereinafter "Sekine") and U.S. Patent 6,051,473 (hereinafter "Ishida").

Claim 1 includes a limitation that subsequent to depositing a metal layer, the region of the substrate adjacent to the alignment component has not been doped. Rodder does not teach such a limitation, and therefore claim 1 is patentable over Rodder, Sekine, and Ishida. More specifically, Rodder teaches doping a channel region of a substrate after forming raised source/drain regions and using a disposable gate as a means of self alignment to the immediate channel region during channel doping (Column 2, lines 25-27). Specifically, the advantage of the transistor taught by Rodder is that it reduces source/drain junction capacitance by limiting channel doping to the immediate channel region (Column 22, lines 24-31). The purpose of the disposable gate taught by Rodder is to align the doping to the immediate channel region and prevent contamination of the source/drain junction region (Column 4, lines 5-11). Further, Rodder teaches that the channel region is doped after at least partial removal of the disposable gate (Col. 3, line 66-Col. 4, line 11). As such, without employing

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channel doping, the improvement to the transistor taught by Rodder would be ineffective, and the disposable gate taught by Rodder would be unnecessary, since the purpose of the disposable gate is to ensure doping is localized to the channel region. Therefore, since Rodder teaches that the channel region is doped after at least partial removal of the disposable gate, claim 1 includes limitations not taught by Rodder, Sekine or Ishida, and claim 1 is patentable over Rodder, Sekine and Ishida.

Claim 1 further includes a limitation of an alignment component consisting of a single material. Although Ishida teaches a reserved gate region oxide formed on a substrate (Column 6, lines 38-59), Rodder specifically teaches that a two material disposable gate is necessary to avoid damage to the channel region of the substrate (Column 3, lines 53-65). The use of a two material disposable gate as taught by Rodder may also be necessary for proper channel doping (Col. 3, line 66-Col.4, line 2). As noted above, the disposable gate taught by Rodder is included to ensure proper channel doping alignment (Col. 2, lines 25-31). Therefore, because the transistor taught by Rodder would not be functional, or would be severely damaged when using a one material disposable gate, Rodder teaches away from a combination with Ishida. Specifically, Rodder teaches that the composition of the first and second materials of the disposable gate are chosen such that the second material may be selectively etched with respect to the insulator material and the first material (Col. 3, lines 2-4 and 54-65). Further, Rodder teaches that a two material disposable gate is necessary to avoid sever damage to the channel region (Column 3, lines 64-65). Also, it is inherent that a one material disposable gate would be easier to remove then a two material disposable gate since a one material disposable gate would require only a single step for its removal. Therefore, because Rodder specifically teaches a

two piece disposable gate, and does not mention a one piece disposable gate, the two piece disposable gate in Rodder must be necessary for the functioning and proper fabrication of the transistor taught by Rodder, otherwise Rodder would teach a one material disposable gate. Therefore, Rodder cannot suggest a combination and must teach a way from a combination with Ishida. As a result, claim 1 is patentable over Rodder, Sekine, and Ishida.

Claims 2-12, 16, 29, 30, and 32 depend from claim 1, and therefore include the limitations of claim 1. Since claim 1 is patentable over Rodder, Sekine, and Ishida, claims 2-12, 16, 29, 30, and 32 are also patentable over Rodder, Sekine, and Ishida.

Examiner rejected claims 13-15 and 31 under 35 U.S.C. § 103(a) as being unapentable by Rodder, Sekine and Ishida as applied to claim 1 above, and further in view of U.S. Patent 6,054,355 (hereinafter "Inumiya").

Claims 13-15 and 31 depend from claim 1 and therefore include the limitations of claim 1. Since claim 1 is patentable over Rodder, Sekine and Ishida, claims 13-15 and 31 are patentable over Rodder, Sekine, Ishida, and Inumiya.

Examiner rejected claims 17-19 under 35 U.S.C. § 103(a) as being unapentable by Rodder, Sekine, Ishida and Inumiya as applied to claim 1 and 13 above, and further in view of U.S. Patent 6,051,865 (hereinafter "Gardner").

Claims 17-19 depend from claim 1 and therefore include the limitations of claim 1. Since claim 1 is patentable over Rodder, Sekine, Ishida, claims 17-19 are therefore patentable over Rodder, Sekine, Ishida, Inumiya, and Gardner.

Examiner rejected claim 28 under 35 U.S.C. § 103(a) as being unaptable by Rodder, Sekine and Ishida as applied to claim 1 above, and further in view of "Silicon Processing for the VLSI ERA" Volume 2 (hereinafter "Wolf").

Claim 28 depends from claim 1 and therefore includes the limitations of claim 1. Since claim 1 is patentable over Rodder, Sekine, and Ishida, claim 28 is patentable over Rodder, Sekine, Ishida, and Wolf.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Arlen M. Hartounian at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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